Multi Level Inverters: A Review Report

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Abstract-**Multilevel converters are increasingly being considered for high power applications because of their ability to operate at higher output voltages while producing lower levels of harmonic components in the switched output voltages. Two well known multilevel converter topologies are the Neutral Point Clamped (NPC) Inverter and Cascaded inverter. One of the major problems in electric power quality is the harmonic contents. There are several methods of indicating the quantity of harmonic contents. The most widely used measure is the total harmonic distortion (THD). Various switching techniques have been used in static converters to reduce the output harmonic content. Pulse Width Modulation techniques for multilevel inverters have been developed very intensively in recent years. Many carriers based and sinusoidal PWM (SPWM) techniques for multilevel inverters have been properly deduced from that of two-level inverter. In contrast, PD modulation of a NPC inverter is harmonically superior, because it places harmonic energy directly into the carrier harmonic for each phase leg, and relies on cancellation of this harmonic across phase legs as the line-to-line voltage is developed. Many different PWM-strategies for multi-level inverters exist. This paper proposes the various multi level circuits with SPWM strategies for Inverters. Operating principles with switching functions are analyzed for Five to fifteen (odd) levels SPWM inverter. Five-level to fifteen level (odd levels) SPWM inverter is presented to alleviate harmonic components of output voltage.**

Index Terms-**Multilevel Inverter, Diode clamped, H-Bridge, Capacitor Clamped, DC/AC converters, Inverters.**

1. INTRODUCTION

In general, increasing the switching frequency in voltage source inverters (VSI) leads to the better output voltage / current waveforms. Harmonic reduction in controlling a VSI with variable amplitude and frequency of the output voltage is of importance and thus the conventional inverters which are referred to as two-level inverters have required increased switching frequency along with various PWM switching strategies. In the case of high power / high voltage applications, however, the two-level inverters have some limitations to operate at high frequency mainly due to switching losses and constriction of device rating itself. Moreover, the semiconductor switching devices should be used in such a manner as problematic series / parallel combinations to obtain capability of handling high power. Nowadays the use of multilevel approach is believed to be promising alternative in such a very high power conversion processing system. Advantages of this multilevel approach include good power quality, good electromagnetic compatibility (EMC), low switching losses, and high voltage capability.

2. MULTILEVEL CONCEPT

Recent advances in power electronics have made the multilevel concept practical. In fact, the concept is so advantageous that several major drives manufacturers have obtained recent patents on multilevel power converters and associated switching techniques. It is evident that the multilevel concept will be a prominent choice for power electronic systems in future years, especially for medium-voltage operation.

Multi-level inverters are the modification of basic bridge inverters. They are normally connected in series to form stacks of level.

The topological structure of multilevel inverter must cope with the following points.

1) It should have less switching devices as far as possible.

2) It should be capable of enduring very high input voltage such as HVDC transmission for high power applications.

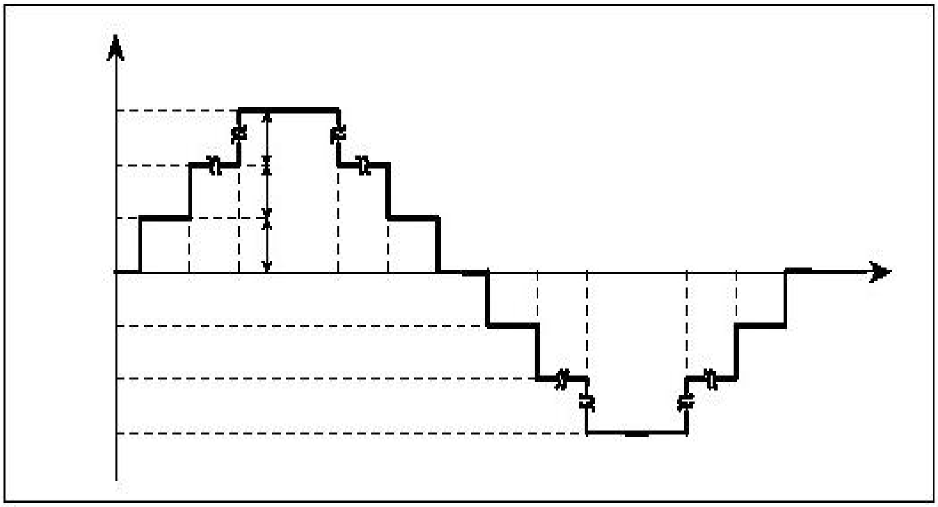
3) Each switching device should have lower switching frequency owing to multilevel approach.

3. MULTILEVEL TOPOLOGIES

It is a fact that, until today, multilevel topologies are the best alternative to implement low-frequency based inverters with low output voltage distortion. This chapter makes a review about most common multilevel topologies and shows which ones are more suitable to implement inverters for SARES.

The multilevel concept and notation.

A multilevel inverter can be defined as a device that is capable to produce a stepped waveform. The generalized stepped waveform is shown in figure 1.



Usually, and also in this work, the follow definitions apply:

p:number of steps in a quarter-cycle;

2*p + 1: number of levels of a converter;

4*p:number of steps of a converter.

Quarter-Wave Symmetric Multilevel Waveform

The optimized harmonic stepped waveform is assumed to be the quarter-wave Symmetric. The first half cycle of the quarter-wave symmetric waveform is depicted in Fig. 2.

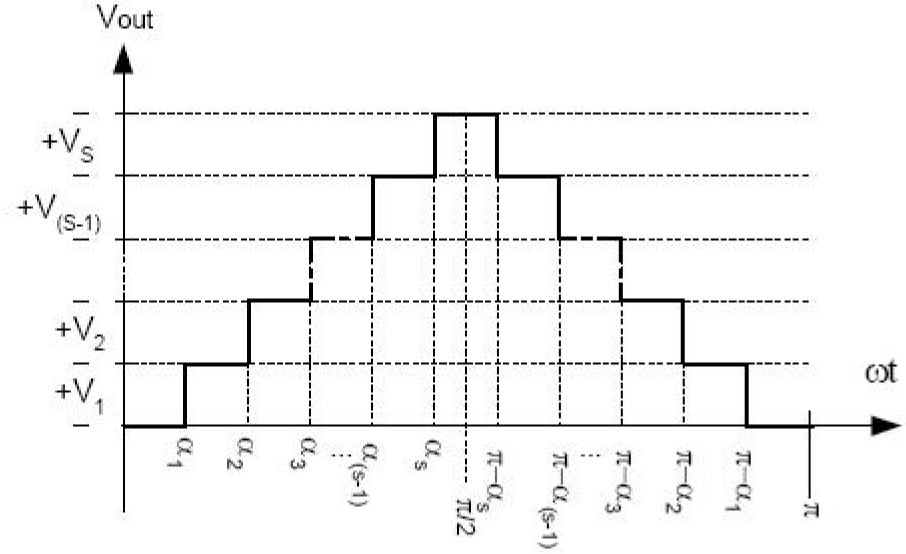


Fig 2. First half cycle of the quarter-wave symmetric waveform

The output voltage level is zero from $\omega t = 0$ to $\omega t = \alpha 1$. At $\omega t = \alpha 1$, the output voltage level is changed from zero to +V1, and from +V1 to +(V1+V2) at $\omega t = \alpha 2$. The process will be repeated until $\omega t = \pi/2$, and the output voltage level becomes +V1 +V2+…+V(S-1)+VS. Then, in the second quarter, the level of output voltage will be decreased to +V1 +V2+…+V(S-1) at $\omega t = \pi-\alpha S$. The process will be repeated until $\omega t = \pi-\alpha 1$ and output voltage becomes zero again. In the second half of the waveform, the process will be repeated all of previous steps except the amplitude of the dc sources change from positive to negative. The next period will then repeat the same cycle.

Fourier Series Analysis

The Fourier series coefficient are given by

$$a_n = \frac{4}{\pi}\int_0^{\frac{\pi}{2}} f(\omega t)\sin(n\omega t)d(\omega t) \qquad \text{,for odd n}$$

$$a_n = 0 \qquad \text{,for even n}$$

$$b_n = 0 \qquad \text{,for all n}$$

$$f(\omega t) = V_{out}(\omega t)$$

For all *n*, the Fourier series is given as

$$f(\omega t) = \sum_{n=1}^{\infty} a_n \sin(n\omega t)$$

$$\text{let } \alpha = \omega t$$

Hence,

$$a_n = \frac{4}{\pi} \int_0^{\frac{\pi}{2}} f(\alpha) \sin(n\alpha) d(\alpha)$$

Finally, the Fourier series of the quarter-wave symmetric parallel connected multilevel waveform is written as follows:

$$v_{out}(\omega t) = \sum_{n=1}^{\infty} \left[\frac{4E}{n\pi} \sum_{k=1}^{S} \cos(n\alpha_k) \right] \sin(n\omega t)$$

Where, *ak* is the switching angles, which must satisfy the following condition

$$\alpha_1, \alpha_2, \ldots, \alpha_S < \frac{\pi}{2} \qquad (1.3.1)$$

Where,

s is the number of H-bridge cells.

n is odd harmonic order.

and *E* is the amplitude of dc voltages.

4. TOTAL HARMONIC DISTORTION (THD) CALCULATION

As introduced in the first chapter, the total harmonics distortion (THD) is mathematically given by

$$THD = \frac{\sqrt{\sum_{n=2}^{\infty} H_{(n)}{}^{2}}}{H_1} \tag{1.4}$$

Where

H_1 is the amplitudes of the fundamental component, whose frequency is w_0

and H_n is the amplitudes of the nth harmonics at frequency nw_0

The amplitude of the fundamental and harmonic components of the quarter-wave symmetric multilevel waveform can be express as:

$$h_n = \frac{4E}{n\pi} \sum_{k=1}^{S} \cos(n\alpha_k) \tag{1.4.1}$$

let $H_{(n)} = h_n$ and $H_1 = h_1$

$$THD = \frac{\sqrt{\sum_{n=2}^{\infty} h_n{}^{2}}}{h_1} \tag{1.4.2}$$

$$THD = \frac{\sqrt{\sum_{n=2}^{\infty} \left(\frac{1}{n} \sum_{k=1}^{S} \cos(n\alpha_k) \right)^{2}}}{\sum_{k=1}^{S} \cos(\alpha_k)} \tag{1.4.3}$$

Therefore, output voltage THD of the presented waveform can be calculated. Theoretically, to get exact THD, infinite harmonics need to be calculated. However, it is not possible in practice. Therefore, certain number of harmonics will be given. It relies on how precise THD is needed. Usually, $n = 63$ is reasonably accepted.

5. ADVANTAGES OF MULTILEVEL VOLTAGES

In general, multilevel power converters can be viewed as voltage synthesizers, in which the high output voltage is synthesized from many discrete smaller voltage levels. The main advantages of this approach are summarized as follows:

- The voltage capacity of the existing devices can be increased many times without the complications of static and dynamic voltage sharing that occur in series-connected devices.
- Spectral performance of multilevel waveforms is superior to that of their two- level counterparts.
- Multilevel waveforms naturally limit the problems of large voltage transients that occur due to the reflections on cables, which can damage the motor windings and cause other problems.

5. TYPES OF MULTILEVEL CIRCUITS

Multilevel power conversion technology is a very rapidly growing area of power electronics with good potential for further development. The most attractive applications of this technology are in the medium-to high-voltage range (2-13 kV), and include motor drives, power distribution, power quality and power conditioning applications. There are different types of multi level circuits involved. The first topology introduced was the series H-bridge design. This was followed by the diode clamped converter, which utilized a bank of series capacitors. A later invention detailed the flying capacitor design in which the capacitors were floating rather than series-connected. Another multilevel design involves parallel connection of inverter phases through inter-phase reactors. In this design, the semiconductors block the entire dc voltage, but share the load current. Several combinational designs have also emerged some involving cascading the fundamental topologies. These designs can create higher power quality for a given number of semiconductor devices than the fundamental topologies alone due to a multiplying effect of the number of levels.

The most actively developed of multilevel topologies are listed in figure 4.

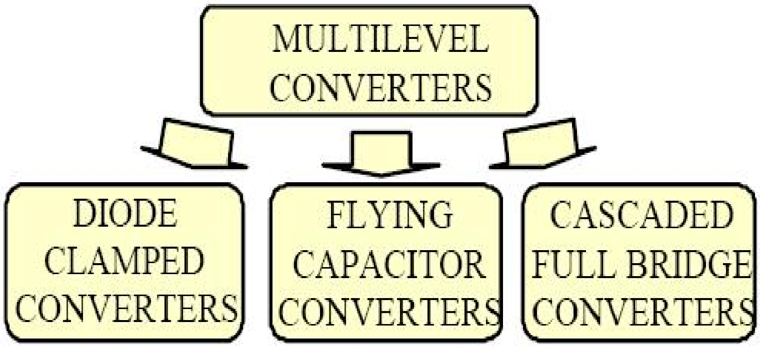


Fig. 4 Multilevel converter topologies.

Diode-Clamped Multilevel Topology

The first practical multilevel topology is the neutral-point-clamped (NPC) PWM topology. The three-level version of this topology, shown in Figure 5(b), has several distinct advantages over the two-level topology.

The advantages are:

- Voltages across the switches are only half of the dc-link voltage.
- The first group of voltage harmonics is centered on twice the switching frequency.

This topology can be generalized, and the principles used in the basic three-level topology can be extended for use in topologies with any number of levels.

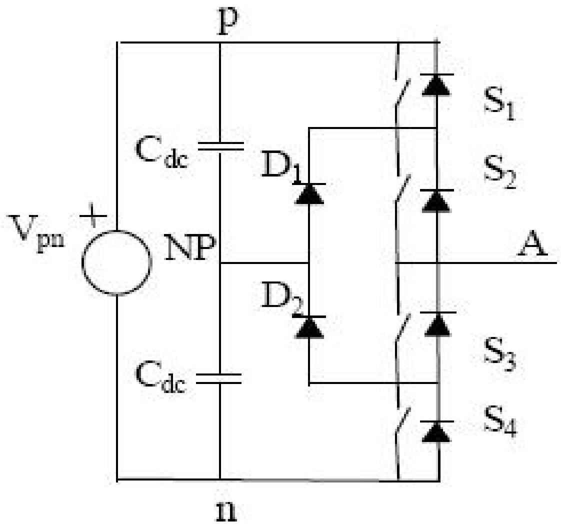
However, practical experience with this topology revealed several technical difficulties that complicate its application for-high power converters.

These are as follows:

- This topology requires high speed clamping diodes that must be able to carry full load current and are subject to severe reverse recovery stress. Although measures to alleviate this problem can be applied, this remains a serious consideration.
- For topologies with more than three levels the clamping diodes are subject to increased voltage stress equal to Vpn.(n-1)/n. Therefore, series connection of diodes might be required.

This complicates the design and raises reliability and cost concerns.

The issue of maintaining the charge balance of the capacitors is still an open issue for NPC topologies with more than three-levels. Although the three-level NPC topology works well with high power factor loads, NPC topologies with more than three levels are mostly used for static var compensation circuits.



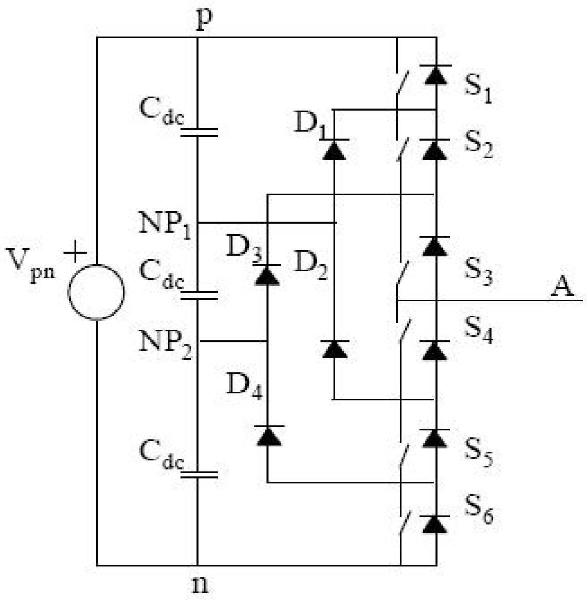


Fig 5 (a) (b) Two-level and Three-level version of Diode clamped topology.

Flying Capacitor Multilevel Topology

The flying capacitor multilevel topology is considered to be the most serious alternative to the diode-clamped topology. Figure 2.3 gives the Three- and Four-level flying capacitor phase leg.

The significant advantage of this topology is that

- It eliminates the clamping diode problems present in the diode-clamped multilevel topologies.
- Additionally, this topology naturally limits the dV/dt stress across the devices and introduces additional switching states that can be used to help maintain the charge balance in the capacitors.

Unlike the diode-clamped converter, the flying capacitor topology has enough switching states to control the charge balance in the single isolated leg with converters having any number of levels, even if the phase current is unidirectional. This makes this topology attractive even for the dc/dc converters. They are:

- The dc-link capacitor charge controller adds complexity to the control of the whole circuit.
- The flying capacitor topology might require more capacitance than the equivalent diode clamped topology.

In addition, it is obvious that rather large rms currents will flow through these capacitors. There is a potential for parasitic resonance between decoupling capacitors.

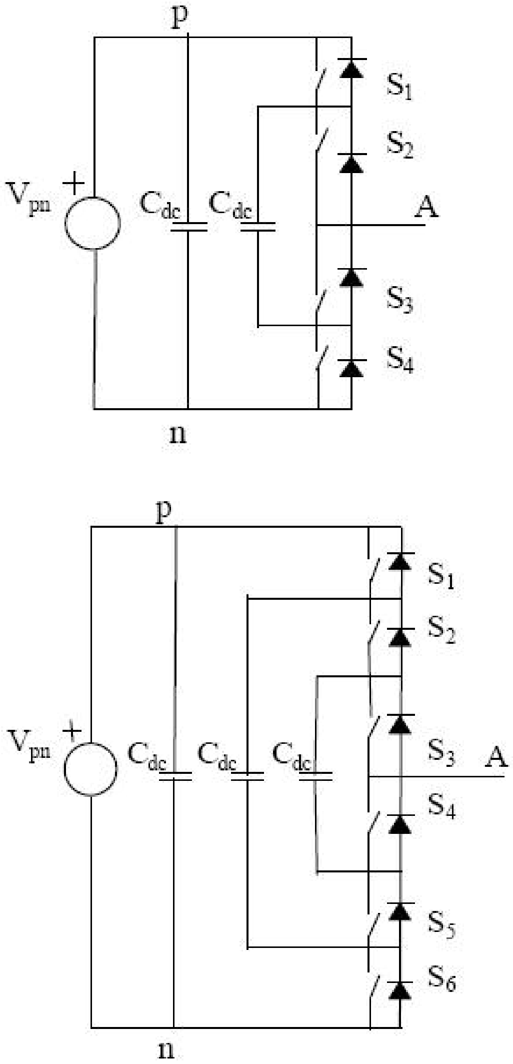


Figure 6 (a) Single Phase Three -level Flying capacitor inverter

(b) Single Phase Four -level Flying capacitor inverter

Multilevel Configurations with Cascaded Two-Level Full-Bridge Inverters

The modularity of this structure allows easier maintenance and provides a very convenient way to add redundancy into the system. The multilevel inverter using cascaded-inverter with separate DC sources synthesizes a desired voltage from several independent sources of dc voltages, which may be obtained from batteries, fuel cells, or solar cells. This configuration recently becomes very popular in ac power supply and adjustable speed drive applications. This new inverter can avoid extra clamping diodes or voltage balancing capacitors. A single-phase m-level configuration of such an inverter is shown in Fig 7.

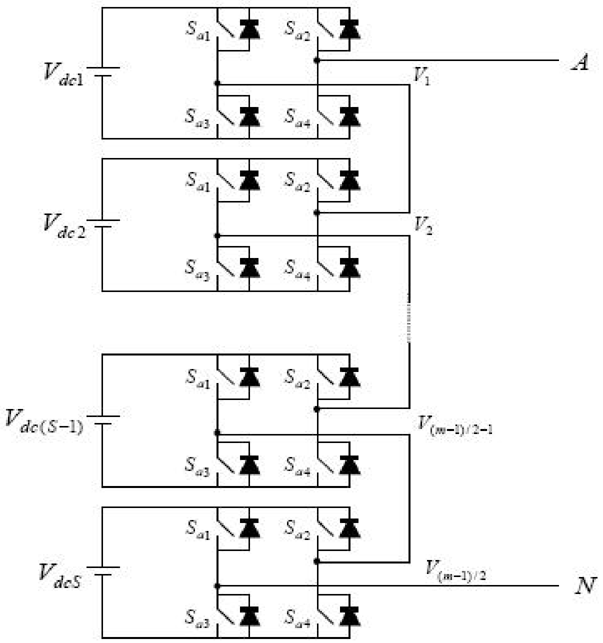


Figure 7. Single Phase cascaded multi-level full-bridge inverter.

One major advantage of this hybrid approach is that the number of output can be further increased without addition of any new components, requiring only the dc sources with different voltage levels.

6. COMPARISON AMONG 3 MULTILEVEL INVERTERS IN APPLICATION ASPECTS

In high power system, the multilevel inverters can appropriately replace the exist system that use traditional multi-pulse converters without the need for transformers. All three multilevel inverters can be used in reactive power compensation without having the voltage unbalance problem. Table 1 compares the power component requirements per phase leg among the three multilevel voltage source inverter mentioned below. It shows that the number of main switches and main diodes, needed by the inverters to achieve the same number of voltage levels. Clamping diodes were not needed in flying-capacitor and cascaded-inverter configuration, while balancing capacitors were not needed in diode clamp and cascaded-inverter configuration. Implicitly, the multilevel converter using cascaded-inverters requires the least number of components.

TABLE 1

COMPARISON OF POWER COMPONENT REQUIREMENTS PER PHASE LEG AMONG THREE MULTILEVEL INVERTERS

Inverter Configuration	**Diode – Clamped**	**Flying – Capacitors**	**Cascaded – inverters**
Main switching devices	2 (m–1)	2(m–1)	2(m–1)
Main diodes	2 (m–1)	2(m–1)	2(m–1)
Clamping diodes	(m–1) (m–2)	0	0
DC bus capacitors	(m – 1)	(m – 1)	(m – 1)/2
Balancing Capacitors	0	(m – 1) (m – 2)/2	0

In very high power application especially with very high input voltage, traditional two-level VSIs could not avoid to sue the series connected semiconductor switches so as to cope with limitations of device rating utilized and it may be very cumbersome and even problematic mainly due to difficulty of device matching deteriorating utilization factor of switching devices. The multilevel topology, however, suggests a good solution for such a problem.

Multilevel converters are increasingly being considered for high power applications because of their ability to operate at higher output voltages while producing lower levels of harmonic components in the switched output voltages. Two well known multilevel converter topologies are the Neutral Point Clamped (NPC) Inverter and cascaded inverters.

To operate a cascade multilevel inverter using a single DC source, it is proposed to use capacitors as the DC sources for all but the first source. Consider a simple cascade multilevel inverter with two H-bridges as shown in Fig. 8.

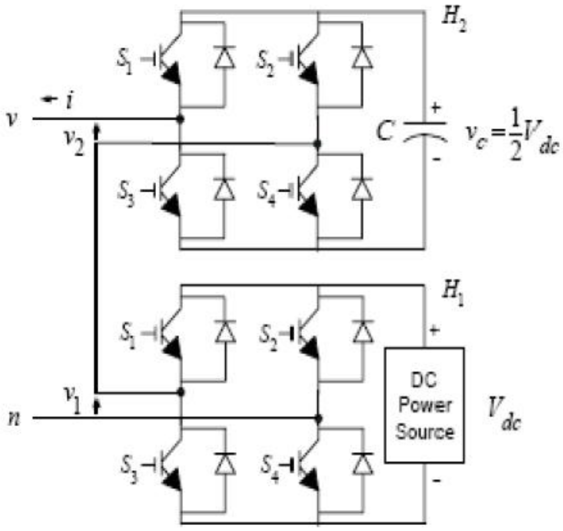


Fig. 8. Single-phase structure of a multilevel cascaded H-bridges inverter.

The DC source for the first H-bridge (H1) is a DC power source with an output voltage of V_{dc}, while the DC source for the second H-bridge (H2) is a capacitor voltage to be held at V_{dc} /2. The output voltage of the first H-bridge is denoted by v_1 and the output of the second H-bridge is denoted by v_2 so that the output of this two DC source cascade multilevel inverter is $v(t)=v_1(t)+v_2(t)$ By opening and closing the switches of H1 appropriately, the output voltage v_1 can be made equal to - V_{dc} , 0, or V_{dc} while the output voltage of H2 can be made equal to - $V_{dc}/2$, 0, or $V_{dc}/2$ by opening and closing its switches appropriately.

The NPC inverter uses a series string of capacitors to subdivide a single high voltage DC bus into the required number of voltage levels, and each phase leg output can be switched to any one of these levels. In comparison the Cascaded inverter uses the series connection of a number of full bridge inverters to construct each multilevel phase leg. The main disadvantage of this topology is that each full bridge inverter requires its own isolated DC supply, which is generally achieved using a multi winding low frequency transformer or high frequency DC to DC converters. The need for these DC supplies has generally restricted the use of Cascaded inverters to the high power range of operation where several output voltage levels are needed and the Neutral Point Voltage balancing problem for a NPC inverter complicates the use of that structure. A further attraction of the Cascaded inverter is that the control and protection requirements of each bridge are modular.

More recently, a new inverter topology (derived from the Cascaded structure) called the Hybrid inverter has been proposed, where the cascaded series inverters have different internal DC bus voltages, use different switching devices (IGCT's and IGBT's) and are modulated quite differently.

Different types and levels of multilevel inverters are shown in bellow

Five level inverter

Assuming that all DC side capacitors have the same voltage *E*, different switching modes provide different output voltages. Table 1 lists five modes for the 5-level diode-clamped multilevel inverter. The voltage *Vout* in the table is the line-to-neutral voltage. The number of inverter level comes from the voltage levels. In every operating mode, four switches are in "on" state and the other four are in "off" state. If the inverter output voltage changes only between two contiguous modes, the main switch voltage and main diode voltage will not exceed *E*. Some of the clamped diodes, however, do need to have higher rating than *E*. For example, the DB2 voltage rating should be 2E. From the five modes switching operation, another advantage of multilevel inverter over the seriesswitches 2-level VSI is that there is no possibility of simultaneous operation of the series switches ("shoot through").

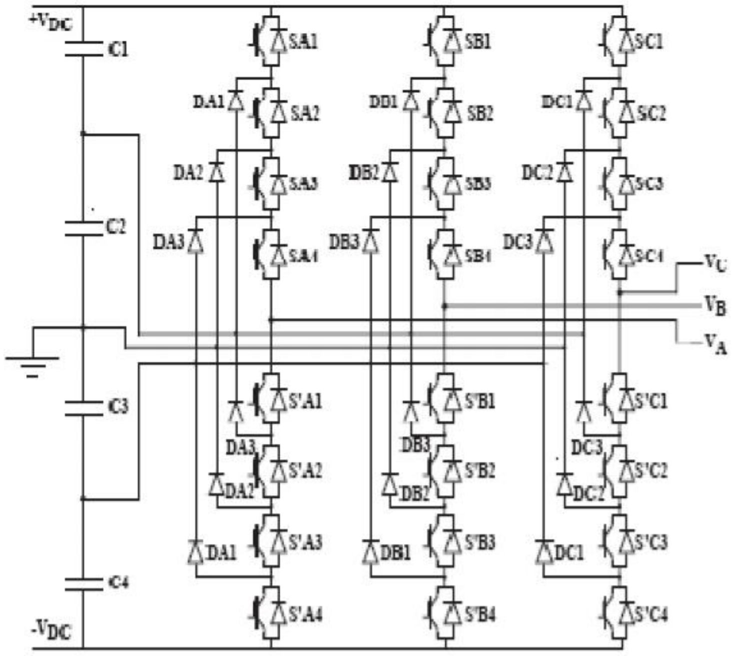


Fig. 9: Five level diode bridge inverter

Switching strategy

The fundamental requirement for the diode-clamped multilevel inverter switching scheme is to ensure that the switches operate in the contiguous modes listed in Table 1. The most popular and simple methods are step modulation and sinusoid pulse width modulation (SPWM). In step modulation, four voltage levels are compared with the sinusoid reference waveform as shown in Figure 10. The result is used to control all the main switches.

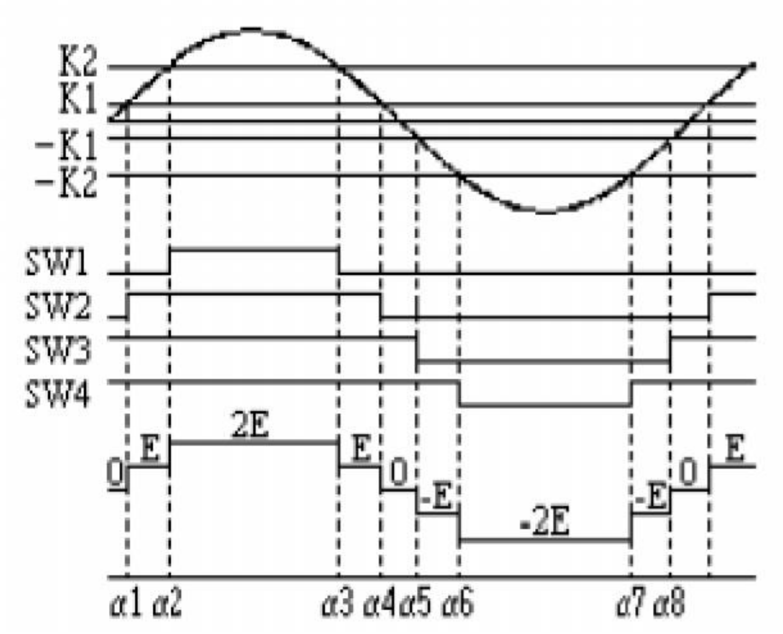


Figure 10. Step Modulation switching strategy.

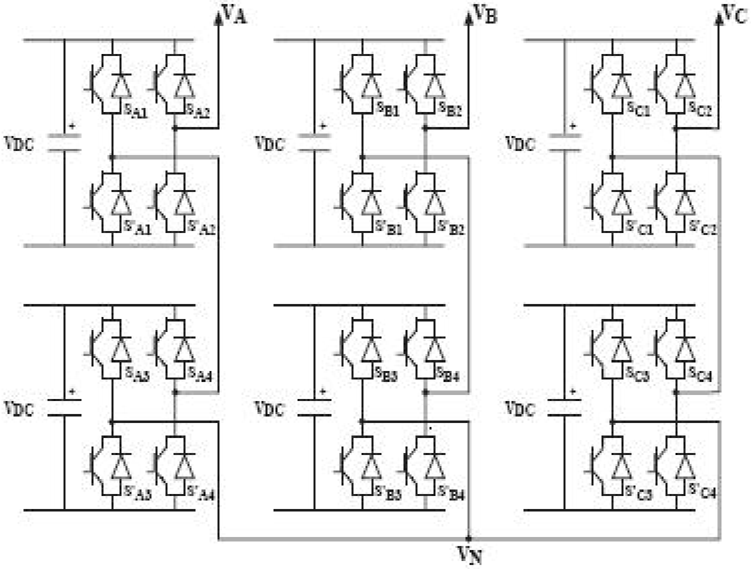


Fig. 11: Five level H-Bridge inverter

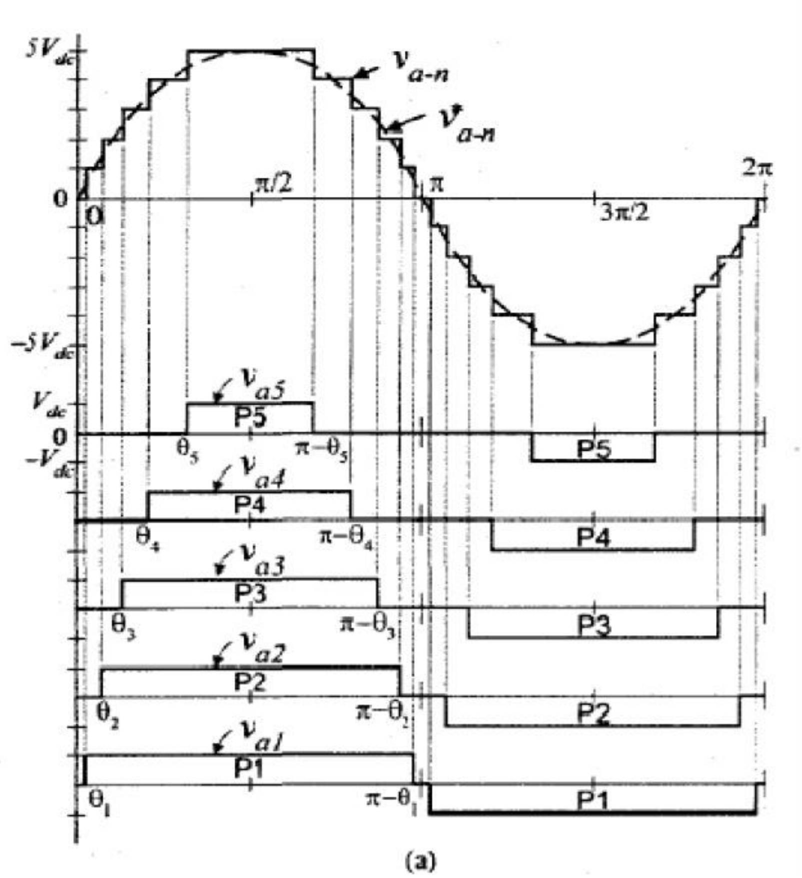


Fig. 12: Switching strategies for five level H-Bridge inverter

Seven level inverter

The advantage of this topology, shown in Figure 13, is a reduction in switch count (36 down to 24 devices for a 7 level inverter) and more effective usage of the natural switching speed and voltage blocking characteristics of the different types of power electronic devices that are required. Furthermore because the number of full bridge inverters required is reduced the design of the multi winding transformer for the DC supplies is considerably simplified.

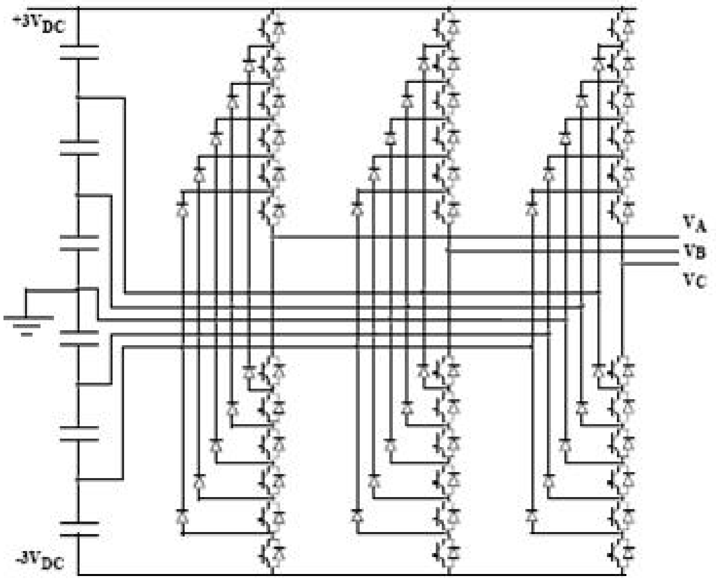


Fig. 13: Seven level diode inverter

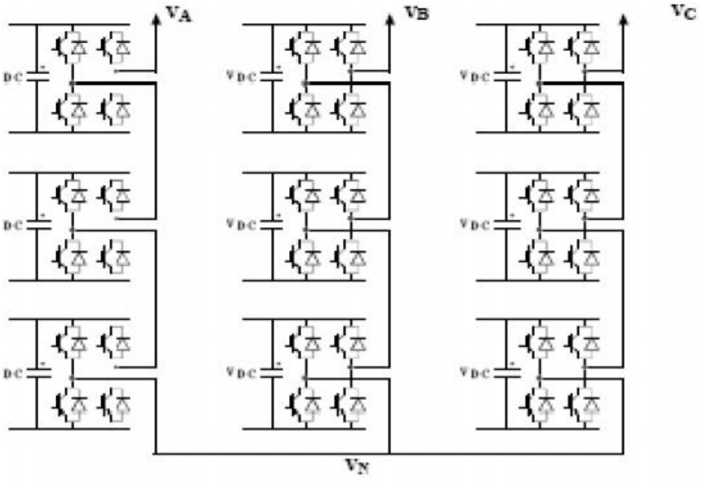


Figure 14 : Structure of a Seven Level Cascaded Inverter.

The DC source for the first H-bridge (H1) is a DC power source with an output voltage of V_{dc}, while the DC source for the second H-bridge (H2) is a capacitor voltage to be held at $V_{dc}/2$. The output voltage of the first H-bridge is denoted by v_1 and the output of the second H-bridge is denoted by v_2 so that the output of this two DC source cascade multilevel inverter is $v(t)=v_1(t)+v_2(t)$ By opening and closing the switches of H1 appropriately, the output voltage v_1 can be made equal to $-V_{dc}$, 0, or V_{dc} while the output voltage of H2 can be made equal to $-V_{dc}/2$, 0, or $V_{dc}/2$ by opening and closing its switches appropriately.

Therefore, the output voltage of the inverter can have the values - $3V_{dc}/2$, - V_{dc} , - V_{dc} /2, 0, V_{dc} /2, V_{dc}, $3V_{dc}/2$, which is seven levels and is illustrated in Fig. 15(a). Table I shows how a waveform can be generated using the topology of Fig. 15.

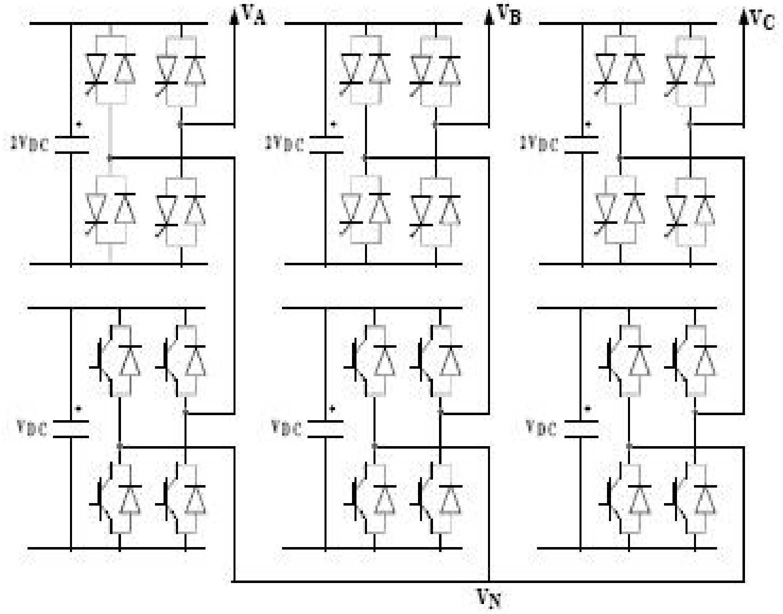


Figure 15: Structure of a Seven Level Hybrid Inverter.

Nine level inverter

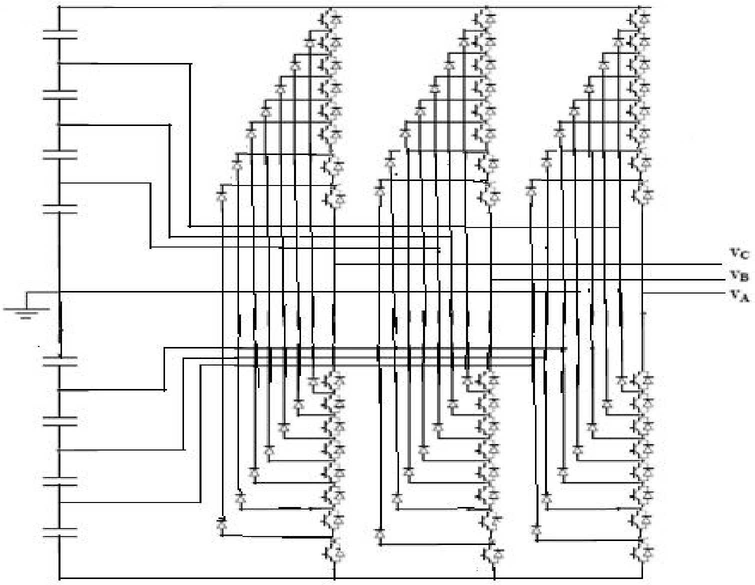


Fig. 16: Nine level diode inverter

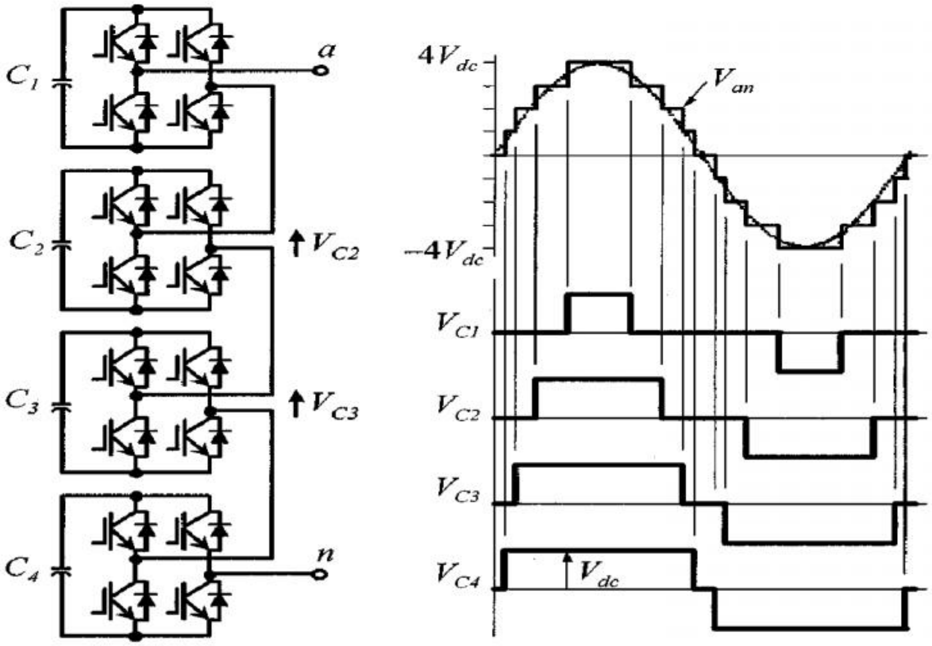


Fig. 17: Nine level H-Bridge inverter and switching strategies

Eleven level inverter

A cascade multilevel inverter consists of a series of H-bridge (single-phase full bridge) inverter units in each of its three phases. Fig. 18 shows an 11-level phase-neutral (2 1- level line-line) cascade inverter connected in a wye configuration. Each H-bridge unit has its own dc source, which for an electric vehicle would be a battery unit.

The combination of the 180° conducting method and the pattern-swapping scheme make the cascade inverter's voltage and current stresses the same and battery voltage balanced. Identical H-bridge inverter units can be utilized, thus improving modularity and manufacturability and greatly reducing production costs.

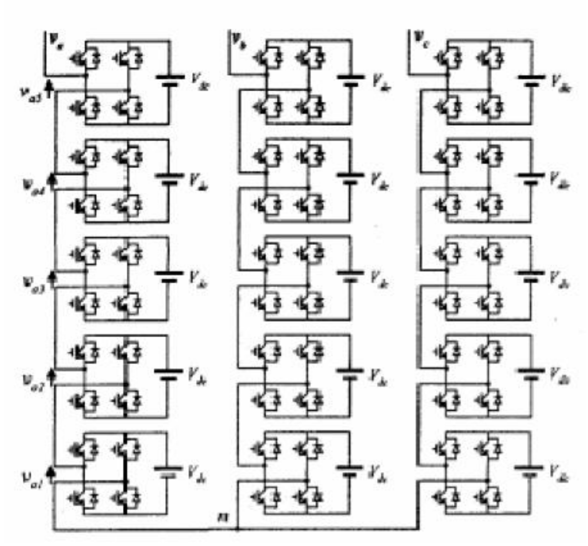


Fig. 18: 1l-level Wye-configured cascade inverter.

Thirteen level inverter

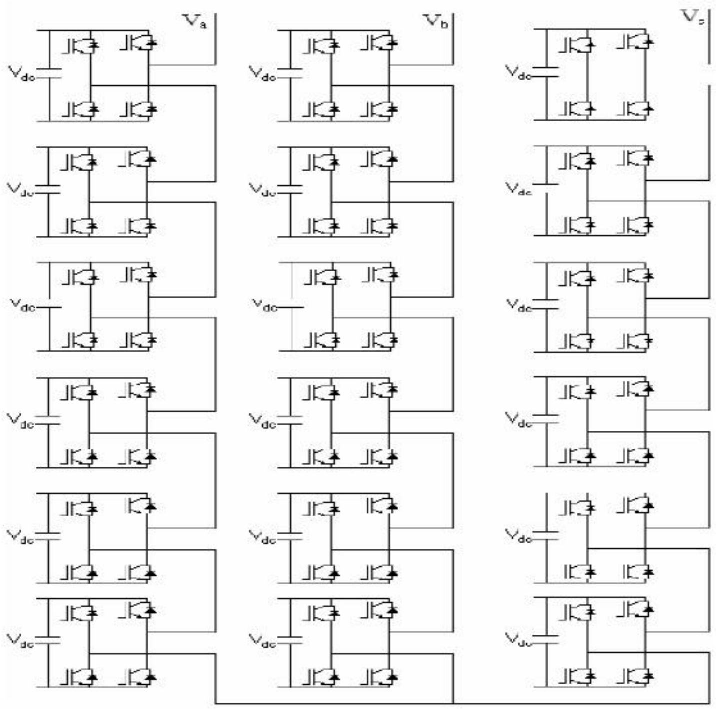


Fig. 19: Thirteen level H-Bridge inverter

Fifteen level inverter

Consider now a 15-level inverter with three H-bridges as shown in Fig. 20. The corresponding waveform is shown in Fig. 21. The DC source for the first H-bridge (H1) is a DC power source with an output voltage of Vdc, the DC source for the second H-bridge (H2) is a capacitor voltage to be held at Vdc/2, and the DC source for the third H-bridge (H3) is a second capacitor voltage held at Vdc/4. As in the 7-level inverter, the capacitor voltages are chosen in this way so that the difference between levels is the same. However, this is not essential. The output voltages of each of the H-bridges are denoted v_1, v_2 and v3 , respectively, so the output voltage of the 15-level inverter is given by $v(t)=v_1(t)+v_2(t)+v_3(t)$. The possible ways in which the voltage waveform of Fig. 21(b) can be achieved are given in Table III.

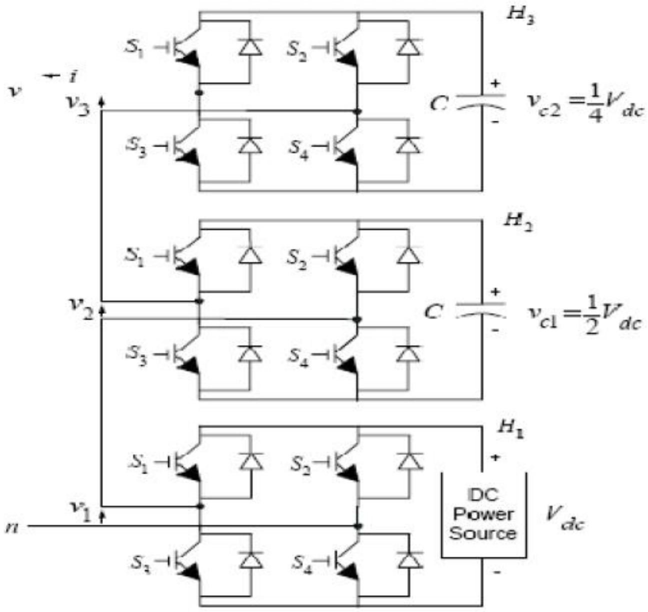


Fig. 20: 15-level (3 DC sources) inverter

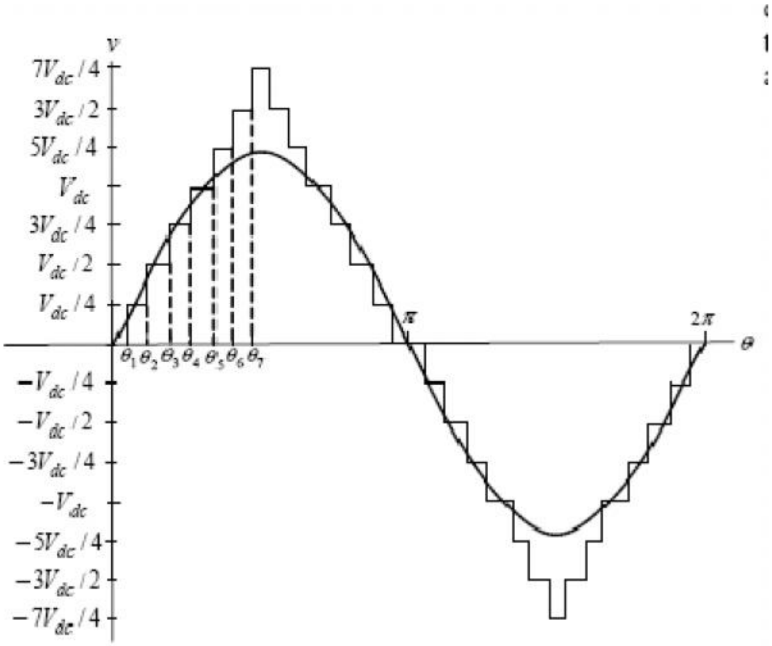


Fig. 21: output voltage waveform for a 15-level inverter.

θ	v_1	v_2	v_3	$v_1 + v_2 + v_3$
$0 \leq \theta \leq \theta_1$	0	0	0	0
$\theta_1 \leq \theta \leq \theta_2$	0		$V_{dc}/4$	$V_{dc}/4$
$\theta_1 \leq \theta \leq \theta_2$	0	$V_{dc}/2$	$-V_{dc}/4$	$V_{dc}/4$
$\theta_1 \leq \theta \leq \theta_2$	V_{dc}	$-V_{dc}/2$	$-V_{dc}/4$	$V_{dc}/4$
$\theta_2 \leq \theta \leq \theta_3$	0	$V_{dc}/2$	0	$V_{dc}/2$
$\theta_2 \leq \theta \leq \theta_3$	V_{dc}	$-V_{dc}/2$	0	$V_{dc}/2$
$\theta_3 \leq \theta \leq \theta_4$	0	$V_{dc}/2$	$V_{dc}/4$	$3V_{dc}/4$
$\theta_3 \leq \theta \leq \theta_4$	V_{dc}	0	$-V_{dc}/4$	$3V_{dc}/4$
$\theta_3 \leq \theta \leq \theta_4$	V_{dc}	$-V_{dc}/2$	$V_{dc}/4$	$3V_{dc}/4$
$\theta_4 \leq \theta \leq \theta_5$	V_{dc}	0	0	V_{dc}
$\theta_5 \leq \theta \leq \theta_6$	V_{dc}	0	$V_{dc}/4$	$5V_{dc}/4$
$\theta_5 \leq \theta \leq \theta_6$	V_{dc}	$V_{dc}/2$	$-V_{dc}/4$	$5V_{dc}/4$
$\theta_6 \leq \theta \leq \theta_7$	V_{dc}	$V_{dc}/2$	0	$6V_{dc}/4$
$\theta_7 \leq \theta \leq \pi/2$	V_{dc}	$V_{dc}/2$	$V_{dc}/4$	$7V_{dc}/4$

TABLE III. OUTPUT VOLTAGES FOR A 15-LEVEL INVERTER

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